LOW-POWER AUDIO CD PLAYER FOR PORTABLE COMPUTERS

Continuing Application Data

This application is a continuation-in-part application under 37 C.F.R § 1.53(b) of application Serial No. 09/595,103, filed June 16, 2000, which claims the benefit of application Serial No. 09/136,207, filed August 19, 1998, now abandoned, which claims the benefit of United States Provisional Patent Application No. 60/079,508 filed on March 26, 1998.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to digital computers and, more particularly, to a digital computer adapted for low power operation while playing an audio CD.

Description of the Prior Art

Portable computers (i.e., notebook, laptop, palmtop and the like) from major original equipment manufacturers such as Toshiba, Compaq, Dell, IBM and others offer CD-ROM drives as either standard or optional devices. Notebook, laptop, palmtop computers are aimed at the mobile computer user who needs or wants to take work home from the office or on a business trip. An added benefit of CD-ROM equipped portable computers is the opportunity to enjoy periods of relaxation and pleasure by playing audio tracks from standard music CDs. In the ensuing discussion, the term notebook computer will be understood to apply also to laptop, palmtop and other portable, battery powered computers.

The Windows operating system's media player or third party audio application can play back standard audio CDs on a portable computer. However the simple function of playing an integral audio CD-ROM requires that the entire notebook system be powered for the duration of the audio play back. This causes excessive drain on the notebook's battery power system,

1 unnecessarily consuming battery energy better saved for CPU intensive use such as word

2 processing and spreadsheet analysis.

3 Conventional laptop and notebook computers typically have several power down modes.

4 They can be powered down such that the CPU is almost completely off, with the state of the

5 CPU saved on a hard drive. A very low power portion of the CPU or an auxiliary circuit (e.g.

6 keyboard controller) is typically used to recognize when a key is pressed. The system then

7 reactivates normal power to allow the CPU to retrieve the stored machine state from the hard

8 drive thereby restoring the computer into an operating mode. Some well known power saving

9 modes are called sleep mode, suspend mode and the like.

10 Consequently, a modern energy efficient computer will, over time, operate in several

11 different power management regimes. For example, if a portable computer is being used in an

12 office environment where electrical power consumption is an insignificant concern, then the

13 computer user may want the computer to provide the highest performance and availability

14 possible. Conversely, if the computer is being operated on battery power where there is no

15 convenient source of electrical energy, then the computer user may want to choose a power

16 management regime for the computer that will maximize the time the computer operates without

17 recharging its batteries, even though performance and availability may be noticeably reduced.

18 To facilitate controlling electrical power consumption in personal computers, Intel

19 Corporation, Microsoft Corporation, and Toshiba Corporation have jointly established an

20 Advanced Configuration and Power Interface Specification ("ACPI Specification"). The ACPI

21 Specification Revision 1.0 of December 22, 1996, Copyright 1996 Intel Corporation, Microsoft

22 Corporation, Toshiba Corporation, establishes both a set of five (5) Global System States G3 -

23 Mechanical Off, G2/S5 - Soft Off, G1 - Sleeping, G0 - Working, S4 - Non-Volatile Sleep, and a

set of four (4) Device Power States D0 - Fully On, through D3 - Off. The ACPI Specification

defines the Global System States as follows.

G3   Electrical power is mechanically turned off.

G2/S5 Electrical power is turned on but the computer consumes a minimal amount of power by not executing either user or system computer programs, and the system's context is not preserved by hardware.

G1   Electrical power is turned on, the system's context is preserved by hardware or system software, but user computer programs are not being executed.

G0   Electrical power is turned on and user computer programs are executed. In the G0 state, devices such as hard disk drives, CD-ROM drives, floppy diskette drives, etc are dynamically turned on and off as needed.

S4   Electrical power may either be turned off, i.e. Global State G3, or turned on with the computer consuming a minimal amount of power, i.e. Global State G2/S5, while system context is preserved in a non-volatile storage file before entering either the G3 or G2/S5 state, thereby permitting the computer to be restored to its prior operating state, i.e. G1 or G0.

The ACPI Specification further defines Device Power States as follows.

D0   The device is completely active and responsive, and consumes the most electrical power.

D1   A lower power state that is defined for different types of devices which preserves more device context than the yet lower power state D2.

D2   An even lower power state than D1 that is again defined f or different types of devices, and which preserves less device context than state D1.

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1   D3   Electrical power is fully removed from the device, device context is lost, and

2   system software must reinitialize the device when it is turned on again.

3   The different computer operating modes and associated power management regimes

4   described above are each characterized by a unique power demand (i.e., current drain) from the

5   battery power supply. This is an important feature both in design of portable computer systems,

6   and in marketing them as well. Great attention is focused on minimizing the power demand for

7   each of the different Global and Device operating modes. Thus, the power demand

8   characterizing each power management regime is a critical factor to be considered for portable

9   computers, particularly one that includes a CD-ROM drive for playing audio CDs.

10   In implementing conventional computer power management strategies, a power

11   management routine ("PMR") executed by the CPU must periodically monitor peripheral

12   devices to assess whether a peripheral device's operation may be suspended. Similarly, if it

13   becomes necessary to access a peripheral device whose operation has been suspended such as in

14   Device Power modes Dl-D3, the PMR must resume that peripheral device's operation.

15   Generally, suspending the operation of a peripheral device and resuming its operation

16   respectively require that the PMR executed by the CPU perform a unique sequence of operations

17   in turning off electrical power to a peripheral device, and in turning electrical power back on.

18   Writing a computer program that detects a need to execute a power-on or a power-off sequence

19   of operations for a peripheral device is a cumbersome task.

20   Previous portable computers that include a CD-ROM use PMR functions to minimize

21   battery drain. However, if CPU operation has been suspended to save electrical power, the

22   computer can essentially do nothing. Therefore, in the minimal power drain mode, the CPU

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1   cannot use the windows operating system's media player or third party audio application to play

2   audio CDs.

3   A significant power drain in portable computers occurs in the conventional LCD monitor.

4   Typically, 60 to 70% of the power consumed by a notebook is consumed by the display. Thus

5   even if a computer's devices, including even perhaps the CPU, were in a lower power state, i.e.,

6   one of the lower Device Power States Dl-D3 for power savings during CD-ROM play only, the

7   need to use the normal LCD to display CD-ROM status and the music playing status would itself

8   impede significantly reducing power consumption.

9   For the reasons described above, it is apparent that a disadvantage of present portable

10   computers for playing audio CDs is that some portion of the computer system must remain

11   energized state to detect key actuation and then to restore power or activate a power restore

12   function of the CPU and associated peripherals (e.g. hard drive, keyboard controller, display,

13   etc.). At times when a portable computer is being used during travel, or when line power is

14   otherwise unavailable, the user may wish to play some audio CDs. Given the limited battery life

15   of most portables, e.g., 3 to 5 hours of use, the user may have to choose to forego using the CD-

16   ROM capability for very long, out of fear that the notebook will not be functional for needed

17   work or communication.

18   **BRIEF SUMMARY OF THE INVENTION**

19   In one embodiment of the invention, a computer system adapted to play an audio CD

20   comprises a computer subsystem and a CD audio subsystem. The computer subsystem

21   comprises a system CPU, a digital-audio generating circuit, a digital computer bus coupling the

22   CPU and the digital-audio generator circuit, and a digital computer bus controller. The CD

23   audio subsystem comprises an audio device capable of playing an audio CD and coupled to the

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1 digital computer bus controller, an audio amplifier circuit coupled to the audio device, and an

2 audio interface coupled to the digital computer bus in parallel to the digital computer bus

3 controller and the audio device. The audio interface is adapted to generate signals to operate the

4 audio device and play the audio CD when power is not being supplied to the computer

5 subsystem.

6 In another embodiment of the invention, a computer system adapted to play an audio CD

7 comprises a computer subsystem and a CD audio subsystem. The computer subsystem

8 comprises a system CPU, a digital-audio generating circuit, a digital computer bus coupling the

9 CPU and the digital-audio generator circuit, and a digital computer bus controller. The CD

10 audio subsystem comprises an audio device capable of playing an audio CD and coupled to the

11 digital computer bus controller, an audio amplifier circuit coupled to the audio device, and an

12 audio interface coupled to the digital computer bus in parallel to the digital computer bus

13 controller and the audio device. The audio interface is adapted to generate signals to operate the

14 audio device and play the audio CD when power is not being supplied to the CPU.

15 In method form, a method for playing an audio CD in a computer system comprises

16 deenergizing a computer CPU; and controlling, using an audio interface coupled to a digital

17 computer bus in parallel to a digital computer bus controller and an audio device capable of

18 playing an audio CD, the audio device and a computer audio amplifier to play an audio CD

19 without supplying energy to the CPU.

20 In a further embodiment, an integrated bus controller comprises a digital bus controller for

21 exchanging commands and data between two or more data buses in a computer system, and an

22 audio interface IC comprising output control logic selectively coupling the IC to at least one of

23 the data buses. The audio interface IC, when coupled to at least one of the data buses, is coupled

1 to at least one of the data buses in parallel with the digital bus controller and is operable to

2 control an audio device capable of playing an audio CD.

BRIEF DESCRIPTION OF THE DRAWINGS

4 FIG. 1 is a block diagram depicting a digital computer in accordance with the present

5 invention having both a computer subsystem and a CD-ROM subsystem that includes an audio-

6 interface IC;

7 FIG. 2 is a block diagram depicting an audio-interface IC in accordance with the present

8 invention;

9 FIG. 3 is a register diagram depicting contents of a register block included in the audio-

10 interface IC illustrated in FIG. 2;

11 FIG. 4 is a state diagram depicting operation of the audio-interface IC illustrated in FIG. 2

12 if the computer subsystem is not energized and is inoperative;

13 FIG. 5 is a flow diagram depicting operation of the computer together with the audio-

14 interface IC illustrated in FIG. 2 when the computer subsystem is energized and the audio-

15 interface IC operates in the third operating mode;

16 FIG. 6 is a block diagram depicting a circuit preferably included in the audio-interface IC

17 for interfacing between a bus included in the computer subsystem of the digital computer and a

18 CD-ROM drive; and

19 FIGS. 7 and 8 are block diagrams of another exemplary embodiment of the present

20 invention, wherein the IC has no transmission gates or MUX circuitry, and the IC is coupled to

21 the IDE bus parallel to the bus bridge.

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DETAILED DESCRIPTION

FIG. 1, depicts a system block diagram of an exemplary battery-powered portable computer 100 adapted for reading digital computer data from a compact disk - read only memory ("CD-ROM"), and for playing audio CDs. For purposes of playing audio CDs and power management, the computer 100 is functionally partitioned into a computer subsystem 104 and a CD-ROM subsystem 106.

The Computer Subsystem 104

The computer subsystem 104 includes all conventional data-processing components such as a microprocessor-based central processing unit and random access memory ("RAM") system ("CPU system") 120 together with various ICs described in greater detail below. The computer 100 also conventionally includes a display 110 (TFT LCD matrix display, CRT and the like), manual input devices 112 (e.g. keyboard, mouse, touch-pad), and read-write mass storage device 114 (e.g. hard drives, floppy drives, optical drives and the like), which operate conventionally within the computer 100.

The computer subsystem 104 includes associated input/output ("I/O") buses (e.g. PCI bus 116, and ISA bus 118) for interconnecting various subsystems included in the computer 100. In the computer 100, the CPU 120 (e.g. a Pentium microprocessor) exchanges data with the PCI bus 116 through a system controller IC 122 (e.g. Intel 82439HX or 82443BX known as the "Northbridge") for controlling on-board L2 cache. The system controller IC 122 is described in a document, a copy of which may be retrieved from http://developer.intel.com/design/chipsets/datashts, which is hereby incorporated by reference. Via suitable adapter devices, conventionally the PCI bus 116 permits the CPU 120 to exchange

1   data with higher performance devices such as the display 110 and the read-write mass storage

2   device 114.

3   A bus bridge IC 124 (e.g. a 82371SB or 82371AB"Southbridge" IC) interconnects the PCI

4   bus 116 with the ISA bus 118 and with an IDE bus 128. A description of the bus bridge IC 124

5   can be obtained from http://developer.intel.com/design/chipsets/datashts and is hereby

6   incorporated by reference. The bus bridge IC 124 is available from Intel Corp., Santa Clara,

7   California. Via suitable adapter devices, conventionally the ISA bus 118 permits the CPU 120 to

8   exchange data with lower speed devices such as the manual input devices 112. However, for

9   particular configurations of the computer 100, the CPU 120 may exchange data with higher

10 performance devices, such as the read-write mass storage device 114, via the ISA bus 118, or

11 directly via the IDE bus 128.

12   A digital-audio generation IC 130 included in the computer subsystem 104 communicates

13 with the CPU 120 either via the ISA bus 118, or via the PCI bus 116 as indicated by a pair of

14 dashed lines 126. The digital-audio generation IC 130 is conventional and may be either a

15 Maestro-1™, Maestro-2™, Maestro-3™, or Allegro™ IC marketed by ESS Technology, Inc. of

16 Fremont, California.

17   As is well known to those skilled in the art, the computer programs executed by the

18 microprocessor included in the CPU 120 of a laptop or notebook computer 100 usually include

19 Power Management Routines (PMRs). Under appropriate operating conditions, the PMRs may

20 place the computer 100 into one of the several power management operating modes such as

21 those described previously for the ACPI Specification. Computer programs that place the

22 computer 100 into one of the various power management operating modes may be prepared by

23 one having ordinary skill in the art, and form no part of the present invention. Each of the

1 various power management operating modes is characterized by a corresponding battery power

2 requirement. For example, the current demand for the ACPI Specification's Device Power States

3 may be those set forth below.

Device Power State	Battery Power Required
D0 - Fully On	Ir1
D1	Ir2 < Ir1
D2	Ir3 < Ir2
D3 - Off	Ir4 < Ir3

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The CD-ROM Subsystem 106

6 The CD-ROM subsystem 106 includes an audio-interface IC 102 in accordance with the

7 present invention, a CD-ROM drive 138, CD-ROM control buttons 142, an icon liquid crystal

8 display ("LCD") 144, a track-number display 147, an audio output amplifier 146, and audio

9 output transducer 148, e.g. speakers or headphones. The CD-ROM control buttons 142, which

10 connect to audio-interface IC 102 via a control-button bus 143, include buttons for playing or

11 pausing an audio CD, for fast-forwarding the audio CD, for rewinding the audio CD, and for

12 stopping or ejecting the audio DC. Thus, the CD-ROM control buttons 142 permit a user of the

13 computer 100 to completely control operation of the CD-ROM drive 138 while playing an audio

14 CD. The CD-ROM drive 138 is a conventional CD-ROM drive capable of operating with

15 conventional ATAPI interface commands provided through an IDE-bus extension 129 which

16 originates at the audio-interface IC 102. The CD-ROM subsystem 106 also includes an audio

17 signals bus 152 that supplies left and right channel stereo audio signals directly to the audio

18 output amplifier 146.

10

1   Depending upon the operating mode of the computer 100, an audio switch 154, which

2   operates in response to control signals received from the audio-interface IC 102, may couple the

3   left and right channel stereo audio signals to the digital-audio generation IC 130 included in the

4   computer subsystem 104. When the computer subsystem 104 is not energized, to reduce

5   electrical power consumption caused by leakage electrical currents in ICs included in the

6   computer subsystem 104:

7   1.   the audio switch 154 electrically isolates the audio signals bus 152 from the CD-

8   ROM drive 138; and

9   2.   the audio-interface IC 102 correspondingly electrically isolates itself from the

10   IDE bus 128.

11   A loudness control-signal line 156 couples a volume control signal from the audio-interface IC

12   102 to the audio output amplifier 146. As described in greater detail below, the audio-interface

13   IC 102 provides a signal to the icon LCD 144 via a LCD-signal line 145 for indicating that the

14   CD-ROM drive 138 is operating. The audio-interface IC 102 provides signals to the track-

15   number display 147 via a track-number-display bus 149 for displaying a track number as an

16   audio CD is played.

17   A System Management Bus ("SMBus") 162 permits the audio-interface IC 102 to

18   exchange commands and data with the computer subsystem 104. Within the computer

19   subsystem 104, the SMBus 162 connects to the ISA bus 118 via a keyboard controller IC 164 as

20   indicated in FIG. 1, or the SMBus 162 may connect directly to the bus bridge IC 124, as

21   indicated by a dashed line 166 in FIG. 1.

22   Both the computer subsystem 104 and the CD-ROM subsystem 106 receive electrical

23   power directly from a battery, not illustrated in any of the FIGS. Depending upon the operating

1 mode of the computer 100 for playing audio CDs, either the CD-ROM subsystem 106 alone, or

2 both the computer subsystem 104 and the CD-ROM subsystem 106 may be energized. If the

3 computer subsystem 104 receives no electrical power, then operation of the CD-ROM drive 138

4 is effected completely within the CD-ROM subsystem 106 with the audio-interface IC 102

5 originating signals for controlling operation of the CD-ROM drive 138. If the computer

6 subsystem 104 is energized and operating, then operation of the CD-ROM drive 138 can be

7 effected, via the audio-interface IC 102, by commands received from a computer program

8 executed by the 120.

9 **Interconnections Between The Computer Subsystem 104**

10 **and The CD-ROM Subsystem 106**

11 The audio-interface IC 102 exchanges commands and data with a computer program

12 executed by the CPU 120 through the IDE bus 128 and the SMBus 162. The computer

13 subsystem 104 also selectively supplies left and right audio signals from the CD-ROM drive 138

14 to the digital-audio generation IC 130 depending upon the operating mode of the computer 100.

15 During operation of the computer 100 in which the computer subsystem 104 is energized and

16 operating, the audio-interface IC 102 relays commands and data between the computer

17 subsystem 104 and CD-ROM drive 138. Commands and data which the computer subsystem

18 104 exchanges with the CD-ROM drive 138 are well known to those skilled in the art.

19 **General Description of The Audio-Interface IC 102**

20 Referring now to a detailed block diagram of the audio-interface IC 102 depicted in

21 FIG. 2, the audio-interface IC 102 includes a state machine 202 which controls overall operation

22 of the audio-interface IC 102. Inclusion of the state machine 202 in the audio-interface IC 102,

23 as contrasted with a programmable controller, provides better performance. The state machine

1 202 connects via an internal bus 204 to a SMBus interface 206, to a register block 208, to a LCD

2 control 212, and to a clock generator 214.

3   The SMBus interface 206, which is coupled to the SMBus 162, issues an interrupt signal

4 from an INTN pin 222 whenever a user of the computer 100 presses any of the CD-ROM control

5 buttons 142. The INTN pin 222 may be advantageously connected to a SMBus alert signal-line

6 of the SMBus 162. Upon receiving a SMBus alert signal, a computer program executed by the

7 CPU 120 can interrogate the register block 208 included in the audio-interface IC 102 via the

8 SMBus 162 to determine which of the CD-ROM control buttons 142 has been pressed.

9   In addition to being coupled to the internal bus 204, the register block 208 is also coupled

10 to an operating-mode bus 226 by which the computer 100 supplies operating mode signals to the

11 audio-interface IC 102 via the operating-mode bus 226 include a reset signal which upon

12 activation causes the audio-interface IC 102 to be reset. The operating-mode bus 226 also

13 supplies a signal to the audio-interface IC 102 that indicates whether the computer subsystem

14 104 is energized. And, the operating-mode bus 226 supplies a signal to the audio-interface IC

15 102 which indicates if the device connected to the IDE-bus extension 129 is a CD-ROM drive.

16 Supplying a signal to the audio-interface IC 102 which indicates whether a CD-ROM drive is

17 connected to the IDE-bus extension 129 avoids a requirement that the audio-interface IC 102

18 first power on and then interrogate a device connected to the IDE-bus extension 129 to

19 determine whether such device is a CD-ROM drive or a hard disk drive. Avoiding this

20 interrogation requirement is particularly advantageous if the computer 100 permits a user to

21 readily interchange a CD-ROM drive for some other device such as a hard disk drive or

22 conversely.

1   As is readily apparent, the CD-ROM control buttons 142, icon LCD 144 and track-

2   number display 147 of the CD-ROM subsystem 106 provide a user of the computer 100 with a

3   self-contained interface for playing audio CDs. To effect this functionality, the audio-interface

4   IC 102 includes control-button logic 232 that receives electrical signals from the CD-ROM

5   control buttons 142 via the control-button bus 143. In response to such signals, the control-

6   button logic 232 may store data into the register block 208, or it may cause a digital volume

7   control 236 to transmit control signals via the loudness control-signal line 156 to the audio

8   output amplifier 146. Similarly, when the computer subsystem 104 is playing an audio CD the

9   LCD control 212 transmits a signal via the LCD-signal line 145 to activate an audio playback

10   icon included in the icon LCD 144. And during such audio CD playback the LCD control 212

11   transmits signals via the track-number-display bus 149 which cause the track-number display

12   147 to display a number that indicates the current track of an audio CD. As described in greater

13   detail below" data indicating the current track number is present in the register block 208.

14   When the computer subsystem 104 is energized, a host IDE interface 242 included in the

15   audio-interface IC 102 couples electrical signals between the IDE bus 128 and the IDE-bus

16   extension 129 via an IDE-signals multiplexer 244 included in the audio-interface IC 102. The

17   electrical signals coupled between the IDE bus 128 and the IDE-bus extension 129 effect

18   exchanges of commands and data between a computer program executed by the CPU 120 and

19   the CD-ROM drive 138. However, if only the CD-ROM subsystem 106 is energized, then the

20   state machine 202 exchanges electrical signals with the IDE-bus extension 129 via the IDE-

21   signals multiplexer 244. And as set forth above, if the computer subsystem 104 is not energized

22   the host IDE interface 242 electrically isolates the audio-interface IC 102 from the IDE bus 128

23   of the computer subsystem 104 to reduce, as much as possible, leakage current flowing from the

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1 CD-ROM subsystem 106 into the computer subsystem 104. Set forth below is a table listing

2 commands in accordance with the ATAPI protocol which the state machine 202 may transmit to

3 the CD-ROM drive 138 via the IDE-signals multiplexer 244 and IDE-bus extension 129.

Command	Opcode
Pause / Resume	4Bh
Play Audio MSF	47h
Stop	1Bh
Read Table of Contents	43h
Request Sense	03h
Read Sub Channel	42h
Test Unit Ready	00h
Lock/Unlock	1Eh
Inquiry	12h
Sleep	E6h

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5   The state machine 202 also transmits a pair of signals from the audio-interface IC 102 via

6 a mode-control signal bus 246. A mode signal supplied by the state machine 202 to the mode-

7 control signal bus 246 indicates that the audio-interface IC 102 is operating for receiving signals

8 from the CD-ROM control buttons 142. An electrical power control signal supplied by the state

9 machine 202 to the mode-control signal bus 246 indicates either that the CD-ROM drive 138 is

10 or has been recently operating, or that the CD-ROM drive 138 has not been operating recently.

11 This signal may be used within the CD-ROM subsystem 106 for appropriately controlling the

12 supply of electrical power to the CD-ROM drive 138 and/or the audio output amplifier 146.

13   During power-on initialization of the computer 100, input signals supplied to the audio-

14 interface IC 102 via the mode-control signal bus 246 respectively select an address for the audio-

15 interface IC 102 on the SMBus 162, and also control whether the state machine 202 transmits the

15

1   signal for controlling the supply of electrical power to the CD-ROM drive 138 and/or the audio

2   output amplifier 146.

3   The audio-interface IC 102 also receives a pair of signals via a mode-set signal bus 248

4   that specify particular hardware characteristics of the CD-ROM subsystem 106. One of these

5   signals specifies which one of two (2) different types of volume control ICs is included in the

6   audio output amplifier 146. The other mode-set signal specifies a particular characteristic for

7   signals transmitted from the audio-interface IC 102 to the track-number display 147 via the

8   track-number-display bus 149.

9   The clock generator 214 included in the audio-interface IC 102 connects to an oscillator-

10   in signal-line 252 and to an oscillator-our signal-line 254. The oscillator-in and -out signal-lines

11   252 and 254 connect to an 8 MHz crystal external to the audio-interface IC 102 that is not

12   separately depicted in any of the FIGs.

Register Block 208

14   FIG. 3 illustrates registers 208a-208h included in the register block 208. Seven high

15   order bits of a low-order byte 208aa of a Chip and Revision ID Register 208a stores a

16   programmable address for the audio-interface IC 102 on the SMBus 162. A high-order byte

17   208ab of the Chip and Revision ID Register 208a stores a revision number for the audio-

18   interface IC 102.

19   Respective states stored in software programmable bits 0, 1, 3, and 5 in a low-order byte

20   of a Control-Buttons Change-Register 208b store data indicating pressing of specific CD-ROM

21   control buttons 142. Bit 208ba0 in the stores data indicating that a rewind button has been

22   pressed. Bit 208ba1 stores data indicating that a fast-forward button has been pressed. Bit

23   208ba3 in the Control-Buttons Change-Register 208b stores data indicating that a stop/eject

button has been pressed. And bit 208ba5 in the Control-Buttons Change-Register 208b stores

data indicating that a play/pause button has been pressed. Software programmable bit 208hb0 of

a high-order byte of an Interrupt Status Register 208h stores data indicating that one of the CD-

ROM control buttons 142 has been pressed, and causes the interrupt signal to be transmitted

from the audio-interface IC 102 via the INTN pin 222. Because buttons 1, 3 and 5 in the

Control-Buttons Change-Register 208b are software programmable, a computer program

executed by the CPU 120 can assign data values, i.e. 0 or 1, to any of them.

A state of bit 208ba7 of the Control-Buttons Change-Register 208b indicates whether the

audio-interface IC 102 is enabled for transmitting the ATAPI protocol commands listed above to

the CD-ROM drive 138. A state of bit 208ca1 in a low-order byte of an Electrical Power

Register 208c enables the audio-interface IC 102 for controlling electrical power to the CD-

ROM drive 138 and to the audio output amplifier 146. If bit 208ca1 is enabled, a state of bit

208ca0 in the Electrical Power Register 208c controls the supply of electrical power to the CD-

ROM drive 138 and audio output amplifier 146.

Respective states stored in software programmable bits 0, 1 and 2 in a low-order byte of a

Command Control Register 208d store data for controlling operation of the audio-interface IC

102 when the computer subsystem 104 is energized. Bit 208da0 in the Command Control

Register 208d stores data which controls whether the audio-interface IC 102 is enabled for

executing a single instance of a function specified, as described above, by data values that are

assigned to bits in the Control-Buttons Change-Register 208b by pressing the CD-ROM control

buttons 142. Bit 208da1 stores data which prevents the audio-interface IC 102 from executing

any function specified by data values assigned by pressing the CD-ROM control buttons 142 to

bits in the Control-Buttons Change-Register 208b. Bit 208da2 stores data which indicates

1 whether the audio-interface IC 102 has executed a single instance of a function specified by data

2 values assigned by pressing the CD-ROM control buttons 142 to bits in the Control-Buttons

3 Change-Register 208b.

4 A bit 208ea0 in a low-order byte of an Operating Mode Register 208e stores data which

5 specifies a specific operating mode of the CD-ROM subsystem 106, i.e. the third operating

6 mode, to be described in greater detail below. When the audio-interface IC 102 operates in the

7 third operating mode, bit 208ea4 in the operating Mode Register 208e stores data which specifies

8 selection of a particular drive, i.e. a master drive or a slave drive, to receive ATAPI protocol

9 commands from the audio-interface IC 102.

10 Bit 208eb1 in a high-order byte of the Operating Mode Register 208e controls application

11 of a clock signal to the state machine 202. When the audio-interface IC 102 operates in the

12 mode in which it merely relays data and ATAPI commands between the IDE bus 128 and the

13 IDE-bus extension 129, to conserve energy bit 208eb1 may be set thereby halting application of

14 the clock signal to the state machine 202.

15 Bits 0-6 of a low-order byte 208ga of a Track Number Register 208g store a track

16 number read from an audio CD while it is being played. Software programmable bits 0-6 of a

17 high-order byte 208gb store a track number displayed on the track-number display 147.

Operating Modes

19 If the computer subsystem 104 is energized and operating, in one operating mode of the

20 CD-ROM subsystem 106 the audio-interface IC 102 transparently relays commands and data

21 between the IDE bus 128 and the CD-ROM drive 138. FIG. 4 depicts states and state transitions

22 of the audio-interface IC 102 for an operating mode of the computer 100 in which the computer

23 subsystem 104 is not energized and is inoperative. When the computer subsystem 104 is not

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1 energized and the CD-ROM subsystem 106 is initially energized, or immediately after the audio-

2 interface IC 102 is reset by a signal received from the operating-mode bus 226, the audio-

3 interface IC 102 enters an initialize state 302 depicted in FIG. 4.

4 A pressing of the play/pause button when the audio-interface IC 102 is in the initialize

5 state 302 causes the audio-interface IC 102 to transition to a play state 304 in which the audio-

6 interface IC 102 transmits commands in accordance with the ATAPI protocol to the CD-ROM

7 drive 138 that cause the CD-ROM subsystem 106 to play an audio CD. If the audio-interface IC

8 102 is in the play state 304, then pressing the stop or eject button, or reaching the end of all the

9 audio CD tracks causes the audio-interface IC 102 to re-enter the initialize state 302 and to

10 return to the beginning of the audio CD.

11 While the CD-ROM subsystem 106 is in the play state 304 playing an audio CD, pressing

12 either the fast-forward or rewind buttons causes the audio-interface IC 102 to enter a fast-

13 forward-or-rewind state 306. In the fast-forward-or-rewind state 306 the audio-interface IC 102

14 transmits commands to the CD-ROM drive 138 that either fast-forward or rewind the audio CD.

15 If the CD-ROM drive 138 completes the fast-forward or rewind command, or reaches the end or

16 beginning of the audio CD track, the audio-interface IC 102 re-enters the initialize state 302.

17 While the CD-ROM subsystem 106 is fast-forwarding or rewinding an audio CD, pressing the

18 play button causes the audio-interface IC 102 to enter the play state 304 and resume playing the

19 audio CD at the beginning of the present track.

20 While the CD-ROM subsystem 106 is in the play state 304 playing an audio CD or in the

21 fast-forward-or-rewind state 306 fast-forwarding or rewinding an audio CD, pressing the pause

22 button causes the audio-interface IC 102 to enter a pause state 308 which pauses operation of the

23 CD-ROM drive 138. If the audio-interface IC 102 is in the pause state 308, pressing the play

1   button causes the audio-interface IC 102 to enter the play state 304 and resume playing the audio

2   CD at the present location in the track, pressing either the fast-forward or rewind buttons causes

3   the audio-interface IC 102 to enter the pause state 308, and pressing the stop button causes the

4   audio-interface IC 102 to enter the initialize state 302.

5   If the audio-interface IC 102 is in the initialize state 302, and a signal has been supplied

6   to the audio-interface IC 102 via the mode-set signal bus 248 which enables the state machine

7   202 for controlling the supply of electrical power to the CD-ROM drive 138 and/or the audio

8   output amplifier 146, and a pre-established two (2) minute interval passes during which none of

9   the CD-ROM control buttons 142 are pressed; then the audio-interface IC 102 enters a sleep

10   state 312. Upon entering the sleep state 312 the audio-interface IC 102 sends an ATAPI protocol

11   sleep command to the CD-ROM drive 138 thereby slowing down a clock included in the CD-

12   ROM drive 138. If the audio-interface IC 102 is in the sleep state 312 and a second, pre-

13   established two (2) minute interval passes during which none of the CD-ROM control buttons

14   142 are pressed, then the audio-interface IC 102 enters a suspend state 314 in which the audio-

15   interface IC 102 transmits a signal via the mode-control signal bus 246 which indicates that the

16   CD-ROM drive 138 has not been operating recently. Electrical circuitry included in the CD-

17   ROM subsystem 106 may use this signal from the audio-interface IC 102 for removing electrical

18   power from both the CD-ROM drive 138 and from the audio output amplifier 146. If the audio-

19   interface IC 102 is either in the sleep state 312 or in the suspend state 314, then pressing any of

20   the CD-ROM control buttons 142 causes the audio-interface IC 102 to re-enter the initialize state

21   302.

22   In addition to the two operating modes described above, the preferred embodiment of the

23   audio-interface IC 102 may be configured to operate a third operating mode. In this third

operating mode the computer subsystem 104 is energized and operating, the audio-interface IC

102 receives commands from the CD-ROM control buttons 142, and stores such commands into

the Control-Buttons Change-Register 208b for subsequent retrieval by a computer program

executed by the CPU 120. The flow diagram of FIG. 5 depicts operation of the computer 100

including the audio-interface IC 102 for playing audio CDs in this third operating mode. Thus as

depicted in FIG. 5, in the third operating mode while a user does not press any of the CD-ROM

control buttons 142 the state machine 202 loops at decision block 372 waiting for one of the CD-

ROM control buttons 142 to be pressed. If any of the CD-ROM control buttons 142 are pressed,

the state machine 202 in processing block 374 sets the bit 208hb0 in the Interrupt Status Register

208h thereby causing the SMBus interface 206 to transmit a SMBus interrupt INTN via the

INTN pin 222 either to the keyboard controller IC 164, or to the bus bridge IC 124. In addition

to transmitting a SMBus interrupt, the state machine 202 in processing block 374 also sets the

appropriate bit in the Control-Buttons Change-Register 208b to indicate which of the CD-ROM

control buttons 142 has been pressed. The computer program executed by the CPU 120 in

processing block 376 responds to receipt of the INTN interrupt by reading the contents of the

Control-Buttons Change-Register 208b, and by then transmitting data to the CPU 120 via the

SMBus 162 that resets the bit 208hb0 of the Interrupt Status Register 208h thereby clearing the

INTN interrupt.

After the computer program executed by the CPU 120 clears the INTN interrupt, the state

machine 202 in decision block 378 determines whether the computer program executed by the

CPU 120 has previously set bit 208da1 in the Command Control Register 208d. If bit 208da1 is

not set, then the state machine 202 in decision block 382 determines whether the computer

program executed by the CPU 120 has previously set bit 208da0 in the Command Control

1   Register 208d. If bit 208da0 is set, then the state machine 202 in processing block 384 transmits

2   to the CD-ROM drive 138 via the IDE-bus extension 129 the ATAPI command(s) which cause

3   the IDE bus 128 to respond appropriately to the pressing of the CD-ROM control button 142. If

4   bit 208da1 has been set, and bit 208da0 has not been set, then the state machine 202 merely

5   passes through processing block 386 without sending any commands to the CD-ROM drive 138.

6   After performing either processing block 384 or processing block 386, the state machine

7   202 in processing block 392 again sets bit 208hb0 in the Interrupt Status Register 208h thereby

8   again causing the SMBus interface 206 to transmit a SMBus interrupt via the INTN pin 222

9   either to the keyboard controller IC 164, or to the bus bridge IC 124. As before, the computer

10   program executed by the CPU 120 in processing block 394 responds to receipt of the INTN

11   interrupt by transmitting data to the CPU 120 via the SMBus 162 that resets bit 208hb0 of the

12   Interrupt Status Register 208h thereby clearing the INTN interrupt. After the computer program

13   executed by the CPU 120 resets bit 208hb0, the state machine 202 returns to decision block 372

14   to resume waiting for one of the CD-ROM control buttons 142 to be pressed.

15   FIG. 6 depicts a preferred circuit for interfacing between the IDE bus 128, the IDE-bus

16   extension 129 and the audio-interface IC 102. While the host IDE interface 242 and the IDE-

17   signals multiplexer 244 of the audio-interface IC 102 may employ conventional IC I/O buffers,

18   such conventional circuits will appreciably delay signals passing through the audio-interface IC

19   102 between the IDE bus 128 and the IDE-bus extension 129. Rather than employing

20   conventional IC I/O buffer circuits for the host IDE interface 242 and the IDE-signals

21   multiplexer 244, the preferred circuit depicted in FIG. 6 employs transmission gates 402

22   interposed between the IDE bus 128 and the IDE-bus extension 129 for selectively either

23   coupling them together, or isolating them from each other. Use of the transmission gates 402

1   rather than conventional IC I/O buffers significantly reduces delay for signals passing through

2   the audio-interface IC 102 between the IDE bus 128 and the IDE-bus extension 129.

3   Analogously to the transmission gates 402, signals that the state machine 202 receives

4   from the IDE-bus extension 129 are also selectively coupled to or isolated from input buffers

5   404 for the state machine 202 by a transmission gates 406 also in response to a signal generated

6   by the state machine 202. Alternatively, signals that the state machine 202 transmits to the IDE-

7   bus extension 129 pass through output drivers 408 when the output drivers 408 are enabled by a

8   control signal supplied by the state machine 202. This preferred configuration for exchanging

9   signals between the state machine 202 and the IDE-bus extension 129 also permits isolating the

10   state machine 202 from input signals on the IDE-bus extension 129 during certain critical events

11   such as when the CD-ROM drive 138 is removed to be replaced by another device that is to be

12   coupled to the IDE bus 128 without removing electrical power from the computer subsystem 104

13   and CD-ROM subsystem 106.

14   The transmission gates 402, input buffers 404, transmission gates 406, and output drivers

15   408 collectively constitute an analog multiplexer that, in the illustration of FIG. 6, is enclosed

16   within a dashed line 412. Enabling operation of the analog multiplexer 412 permits exchanging

17   signals between the IDE-bus extension 129 and either the IDE bus 128 or state machine 202.

18   Disabling operation of the analog multiplexer 412 isolates the IDE-bus extension 129 both from

19   the IDE bus 128 and from the state machine 202. Inclusion of the analog multiplexer 412 in the

20   audio-interface IC 102 permits various IDE devices, such as the CD-ROM drive 138, a hard

21   disk, a Digital Video Disk ("DVD") drive, a ZIP drive, or a Superdisk, to be connected to or

22   disconnected from the IDE-bus extension 129 of a fully operational computer 100.

1   Operation of the analog multiplexer 412 is enabled or disabled by a signal coupled from a

2   multiplexer control 414 included in the audio-interface IC 102. The multiplexer control 414

3   transmits the control signal to the transmission gates 402 and 406 via a transmission-gate-control

4   signal-line 416. For disabling operation of the analog multiplexer 412, the multiplexer control

5   414 receives software data via the SMBus 162. For enabling operation of the analog multiplexer

6   412, the multiplexer control 414 may receive either or both a hardware signal via a touchdown

7   signal-line 418 and/or software data via the SMBus 162. The multiplexer control 414 also

8   receives signals from the state machine 202 via a multiplexer-control-signal selection-bus 422.

9   Signals supplied to the multiplexer control 414 from the state machine 202 via the multiplexer-

10   control-signal selection-bus 422 determine whether operation of the multiplexer control 414 is

11   enabled by the signal supplied via the touchdown signal-line 418, or by data supplied to the

12   multiplexer control 414 via the SMBus 162.

13   Accordingly, as illustrated in FIG. 3 the register block 208 of the audio-interface IC 102

14   which employs the preferred analog multiplexer 412 includes a software programmable bit

15   208ca3 located in the low-order byte of the Electrical Power Register 208c. Setting bit 208ca3

16   activates software data control of the multiplexer control 414 via the SMBus 162, while resetting

17   bit 208ca3 activates hardware enablement of the multiplexer control 414 via the touchdown

18   signal-line 418. To effect software disabling and enabling of the multiplexer control 414, the

19   low-order byte of the Electrical Power Register 208c also includes a software programmable bit

20   208ca2 which if set enables operation of the transmission gates 402 and 406. Conversely,

21   resetting bit 208ca2 disables operation of the transmission gates 402 and 406.

22   When the computer 100 is fully operational with a device connected to the IDE-bus

23   extension 129, using one of the manual input devices 112 a user of the computer 100 may direct

24

1   a computer program executed by the CPU 120 to release the device connected to the IDE-bus

2   extension 129. In response thereto, the computer 100 causes the analog multiplexer 412 to

3   isolate the IDE-bus extension 129 from the remainder of the CD-ROM subsystem 106, and then

4   mechanically releases the device so it may be physically removed from the computer 100. Upon

5   subsequent insertion of a device into the computer 100 and connection of that device to the IDE-

6   bus extension 129, the device becomes mechanically locked into the computer 100, and the

7   audio-interface IC 102 responsive, either the hardware signal or software data, re-couples the

8   IDE-bus extension 129 to the remainder of the CD-ROM subsystem 106 thereby restoring the

9   computer 100 to full operation.

Alternative Exemplary Embodiment

11   Figures 7 and 8 depict block diagrams of another exemplary embodiment of the present

12   invention. The embodiment of Figures 1-6 is directed to an audio interface IC 102 that resides

13   on the IDE bus 128 between the bus bridge IC 124 and the IDE device 138. Transmission gates

14   (402, 406, Figure 6) couple and decouple the IC 102 to and from the IDE bus, depending on the

15   mode of operation detected (i.e., system off, etc.). A MUX is provided to generate IDE

16   commands along the IDE extension bus 129. However, the transmission gates described in the

17   previous embodiment may cause a delay or power drain since communication between the bus

18   bridge IC 124 and the IDE device 138 must go through the IC 102. In the embodiment of

19   Figures 7 and 8, the transmission gates and MUX are removed from the IC 102', and the IC 102'

20   is coupled to the IDE bus 128 parallel to the bus bridge IC 124. In this manner, pin count for the

21   IC 102' is reduced and potential power losses and/or delay is avoided, as will be described

22   below.

1   Referring specifically to Figure 7, the audio interface IC 102' is coupled to the IDE bus

2   128 in parallel to the IDE bus controller 124 (which, as described above, is a subset of the bus

3   bridge IC 124), and both are coupled to the IDE device 138 (e.g., CD drive, DVD drive, or other

4   IDE media device). In a first operating mode in which the computer subsystem 104 is energized

5   and operating, the IC 102' of this exemplary embodiment does not relay commands and data

6   between the digital computer bus 128 of the computer subsystem 104 and the CD-ROM drive

7   128, rather the audio interface IC 102' is isolated from the IDE bus 128. Since the IC 102' is

8   isolated from the bus controller, the present embodiment achieves low power loss at the IC 102'

9   (power loss which is largely attributable to negligible leakage current). Moreover, since the IC

10   102' is no longer in the signal path between the bus controller and the device, signal delay is

11   avoided. Thus, the IC 102' of this embodiment is not directly in the transmission path between

12   the device 138 and the controller 124. In the second operating mode in which the computer

13   subsystem 104 is not energized and is inoperative, IC 102' autonomously responds to signals

14   received from the CD-ROM/DVD control buttons and transmitting commands to the IDE device,

15   the commands causing the IDE device to play an audio CD present in the IDE drive, in a manner

16   similar to the previous embodiment.

17   Figure 8 depicts a detailed block diagram of the audio interface IC 102' of this exemplary

18   embodiment. Instead of transmission gates and MUX circuitry of the previous embodiment, this

19   embodiment includes IDE output control logic 502 which couples/decouples the IC 102' to/from

20   the IDE bus 128 according to the overall topology of Figure 7. IDE output control logic

21   generates IDE commands and data to the IDE bus, and receives IDE commands and data from

22   the IDE device. Otherwise, the components of the IC 102' are the same as the IC 102 described

23   above in the previous embodiment.

1   Most computer systems, especially portable systems, are migrating to 3.3 Volt

2   technology. In such systems, chipsets and controllers include 3.3 V operability, but since most

3   peripheral devices (e.g., IDE drives, etc.) still require 5 V power, the 3.3 V devices must be

4   backward-compatible with 5 V systems. For example, newer IDE controllers that support Ultra

5   DMA transfer mode use 3.3 V signaling. To support legacy 5 V devices, 5 V tolerance is

6   required in the 3.3 V controller. As is understood in the art, components of this type are

7   protected using, for example, ESD (electrostatic discharge) technology, wherein a diode (ESD

8   diode) is coupled in reverse bias with respect to a 5 V power rail. Common ways to ensure 3.3

9   V components have 5 V tolerance are: 1) coupling an additional 5 V power rail to the ESD diode

10   or 2) using floating well methodology (which does not require using the ESD diode).

11   For the topology of Figure 7, when the IDE controller is not energized, the IC 102' can

12   still be powered up even if the IDE controller is off. If the IDE controller is utilizing ESD diode

13   protection circuitry, then the 5 V rail is supplied to the controller. If the IC 102' is driving the

14   IDE bus using 3.3 V and the ESD diode is biased with 5 V, then no leakage current will exist in

15   the IDE controller. If the IDE controller is utilizing a floating well protection scheme, then there

16   is no need to have a 5 V rail supplied to the controller. Thus, the system of this embodiment

17   may comprise a power switch (e.g., included with buttons 142) that delivers a 5 V rail to the IDE

18   bus controller, if the system designer is utilizing ESD diode protection. Essentially, a power

19   switch would turn on a 5 V rail in the IDE controller, turn on the IDE device, turn on the audio

20   interface IC 102' and turn on the relevant portions of the CDROM subsystem 106.

21   Those skilled in the art will recognize that numerous modifications may be made to the

22   embodiments described herein. For example, it may be desirable to integrate the IC 102 or the

23   IC 102' of the present invention directly into the bus bridge IC 124. In such a configuration, the

27

1 bus bridge IC 124 would be adapted with additional pins to support the data input/output and

2 functionality of the IC 102 or 102' as described above. In the case of the IC 102', fewer pins

3 would be required since the IC 102' does not require an output IDE bus 129 extension as in the

4 case of IC 102. In yet a further alternative embodiment, the IC 102' may include transmission

5 gates (described above with reference to IC 102), for example, to further limit power loss at the

6 IC and/or specific bus isolation is desirable for a given application. Such transmission gates may

7 either be implemented in place of the output control logic 502, or else be a component of the

8 output control logic 502. Those skilled in the art will further recognize that although the

9 exemplary embodiments have been described herein with reference to conventional IDE

10 controllers and bus controller technology, the present invention is equally applicable to other

11 conventional and/or proprietary bus technologies known in the art.

12   Although the present invention has been described in terms of the presently preferred

13 embodiment, it is to be understood that such disclosure is purely illustrative and is not to be

14 interpreted as limiting. Consequently, without departing from the spirit and scope of the

15 invention, various alterations, modifications, and/or alternative applications of the invention will,

16 no doubt, be suggested to those skilled in the art after having read the preceding disclosure.

17 Accordingly, it is intended that the following claims be interpreted as encompassing all

18 alterations, modifications, or alternative applications as fall within the true spirit and scope of the

19 invention.